What is claimed is:

1. A delay adjustment circuit comprising:

a first gate array for carrying out fine adjustment of the delay time interval that has each gate serially connected;

capacitance connected to the output side of a specified gate in the first gate array via a first switching device;

a second gate array that is connected to the output side of said first gate array via a second switching device and carries out rough adjustment of the delay time interval of said input signal; and

a control device that controls a first switching device and a second switching device so as to adjust the delay time interval of said input signal by adjusting the capacitance connected to the output side of the specified gate in the first gate array and the number of gate stages in the second gate array.

2. A delay adjustment circuit according to claim 1, wherein said control device being provided on board the semiconductor integrated circuit device, being formed to include a register that can set an output value that depends on an internal signal, and adjusting the gate output load and the number of gate stages in said second gate array by switch controlling said first and second switching device based on the register value set in said register.

3. A delay adjustment circuit according to claim 1, wherein said control device being provided on board the semiconductor integrated circuit device, being formed to include a register that can set the output value externally by initialization, and adjusting the gate output load and the number of gate stages in said second gate array by switch controlling said first and second switching device based on the register value set in said register.

4. A clock generating circuit comprising:

the delay adjustment circuit according to any of claims 1 into which a reference clock is input; and

a logic circuit that carries out logical operations on the output signal of the delay adjustment circuit according to one or more of Claims 1 through 3, and outputs a clock having an operational frequency N times said reference clock.

5. A semiconductor integrated circuit device comprising:

the clock generating circuit according to claim 4; and

flip flops that are provided between logic gates and operated at the timing of a specified adjustable edge in said clock generating circuit.

6. A clock generating circuit comprising:

the delay adjustment circuit described in any of Claim 1 through Claim 3 into which a reference clock is input;

logic circuit that carries out logical operation on a reference clock and the output signal of the delay adjustment circuit according to any of Claims 1 through 3 and outputs a clock having an operational frequency N times that of said reference clock; and

a setting device that fixes the output of the delay adjustment circuit according to claim 1 to a constant value only during the non-operational mode; and

wherein a clock is output that has an operational frequency that is equal to that of the reference clock when serving as the non-operational mode or N times the reference clock when serving as the operational mode based on the result of the logical processing of said logic circuit.

7. A clock generating circuit comprising:

the delay adjustment circuit according to claim 1;

a duty ratio detecting device that detects the duty ratio of the clock output of this clock generating circuit; and

a control device that automatically updates the register value in said delay adjustment circuit so as to become a pre-set duty ratio based on the detected output of said duty ratio detecting device.

8. A clock generating circuit comprising:

the delay adjustment circuit according to Claim 2;

a clock skew detecting device that detects clock skew; and

a control device that automatically updates the register values in said delay adjustment circuit so that the clock skew becomes a pre-set expected value based on the detected output of said clock skew detecting device.

9. A clock generating circuit comprising:

one or more delay adjustment circuits having a delay time interval that can be adjusted by the internal register values, the values of the internal memory, and an internal logic signal in the semiconductor integrated circuit device, or an external logic signal; and

a logic circuit that outputs a clock having a desired frequency by carrying out logic operations on one or more signals, these signals being the input signals that have been delayed a specified time interval by said one or more of the delay circuits.

10. A clock generating circuit comprising:

first, second, and third delay adjusting circuits having a delay time interval that can be adjusted by the value of an internal register, the value of the internal memory, and the internal logic signal of the semiconductor integrated circuit device, or an external logic signal;

a first selector that is connected to the input terminals of said three delay adjustment circuits in common and that selects the input of said three delay adjustment circuits or the output of the second delay adjustment circuit depending on one of both of the outputs of the first and third delay adjustment circuits;

a second selector that selects the output of said first or third delay adjustment circuits depending on one or both of the input signal of said three delay adjustment circuits or the output of the second delay adjustment circuit; and

a logic circuit that finds the exclusive AND of the output signals of said first and second selectors.

11. A clock generating circuit comprising:

a first, second, third, and fourth delay adjusting circuits having a delay time interval that can be adjusted by the value of an internal register, the value of the internal memory, and the internal logic signal of the semiconductor integrated circuit device, or the external signal;

a first selector that is connected to the input terminals of the four delay adjustment circuits in common and that selects the output of the first and third delay adjustment circuits depending on one of both of the outputs of the second and fourth delay adjustment circuits;

a second selector that selects the output of the second or fourth delay adjustment circuits depending on one or both of the output signal of the first and third delay adjustment circuits; and

a logic circuit that finds the exclusive AND of the output signals of the first and second selectors.